Claims 1 and 2 remain in the application.

In item 4 on pages 2 and 3 of the above-identified Office action, claim 1 has been rejected as being fully anticipated by Fifield et al. (U.S. 5,022,006; hereinafter "Fifield") under 35 U.S.C. § 102.

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and, therefore, the claims have not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, an integrated memory, including:

bit lines;

word lines intersecting said bit lines at points of intersection;

memory cells disposed at said points of intersection between said word lines and said bit lines;

at least one reference word line intersecting said bit lines at points of intersection;

reference cells disposed at said points of intersection between said at least one reference word line and said bit lines, said reference cells generate a reference potential on said bit lines before an access operation to one of said memory cells;

a redundant word line intersecting said bits lines at points of intersection;

redundant memory cells disposed at said points of intersection between said redundant word line and said bit lines; and

a programmable activation unit having a programming state governing if said redundant word line connected to said redundant memory cells replaces one of said word lines connected to said memory cells or said at least one +reference word line connected to said reference cells during operation of the integrated memory.

The invention of the instant application as set forth in claim 1 provides an integrated memory that has the option of choosing whether the redundant word lines is to be used for

replacing one of the normal word lines or to be used for replacing one of the reference word lines.

As outlined in the specification of the instant application, the practice of providing integrated memories with redundant memory cells connected to redundant word lines for the purpose of repairing faults is generally known in the prior art. By programming an appropriate logic unit, it is, for example, possible for the redundant word line having the redundant memory cells connected thereto to replace one of the normal word lines having the memory the memory cells connected thereto on an address basis during operation of the memory.

Fifield completely supports such a view by stating that the application of memory cell redundancy to enhance the yield of semiconductor memory arrays during the early stages of mass production is extensively practiced throughout the semiconductor industry. See, i.e., Fifield at col. 1, lines 15 to 18. Furthermore, Fifield at col. 5, lines 8 to 21, discloses:

> Defective portions (defined along a respective main memory wordline) of the main memory array, are "replaced" by a good portion (defined along a respective redundant memory wordline) in a redundant array. To accomplish this, the address of each defective main memory wordline

> is programmed into a redundant word decoder (using laser-blown fuses, electrically blown fuses, etc.) to become associated with a unique substitute word line in the redundant array. The redundant word decoder compares incoming address signals with the programmed defective addresses and if a match is found to occur, the redundant word decoder performs its switching operation to select the appropriate redundant word line as a substitute.

However, "[t]he choice of using redundancy by programming the redundant word decoders with the addresses of defective main memory wordlines . . . imposes an additional [disadvantageous] constraint upon the operation of the memory device which directly [a]ffects the memory access time." Fifield at col. 5, lines 22 to 26. In order to solve this memory access time problem, Fifield suggests, among other counter-measures, the use of redundant cells of the type referred to as a twin cell, because each cell is composed of two single device memory cells that store data signals complementary to each other. "One of the reasons for using a twin cell is that the wordline redundancy scheme described [by Fifield] disables the normal drive circuits for the reference cells." Fifield at col. 6, lines 3 to 9. The general structure of the memory according to Fifield is shown in FIG. 1 therein.

Significantly, however, Fifield teaches the replacement of normal memory cells only. Fifield does not contain any hint, let alone actually disclose, the replacement of reference cells.

In contrast to Fifield, the invention of the instant application discloses an integrated memory that has the option of choosing whether the redundant word lines it to be used for replacing one of the normal word lines **or** to be used for replacing one of the reference word lines. Therefore, the invention of the instant application permits a redundant word line and the redundant memory cells and faults in reference cells or faults on the normal word lines or reference word lines connected thereto. Such a configuration results in a significantly greater flexibility in the use of word line redundancy.

As outlined in the specification of the instant application, if, by contrast, it was desirable to provide separate redundant word lines first for repairing faults on the normal word lines and, second, for repairing faults on one of the reference word lines, the integrated memory would need to have a greater number of redundant word lines than the memory according to the invention of the instant application. This is because the invention of the instant application is based upon recognition of the fact that, although a memory has a

large number of normal word lines, it has only an extremely small number, namely, one or two, for example, of reference word lines for each memory block. The probability of one of the reference word lines having a fault is, therefore, much lower than that of a fault arising on one of the normal word lines. Therefore, providing separate redundant word lines to repair the normal word lines, in the first instance, would be ineffective. By providing a common redundant word line for selectively repairing one of the normal word lines or one of the reference word lines, the number of redundant word lines can, therefore, be kept relatively small in the case of the instant application. Thus, the space requirement is likewise small.

Clearly, Fifield does not show the integrated memory as recited in claim 1 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

Finally, applicant appreciatively acknowledges the Examiner's statement that claim 2 "would be allowable if rewritten in

independent form including all of the limitations of the base claim and any intervening claims." In light of the above, applicants respectfully believe that rewriting of claim 2 is unnecessary at this time.

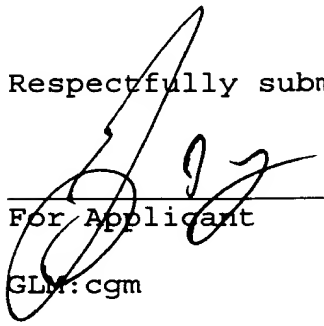
In view of the foregoing, reconsideration and allowance of claims 1 and 2 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

Petition for extension is herewith made. The extension fee for response within a period of one (1) month pursuant to Section 1.136(a) in the amount of $110.00 in accordance with Section 1.17 is enclosed herewith.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



For Applicant

Gregory L. Mayback
Reg. No. 40,719

GLM:cgm

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Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101